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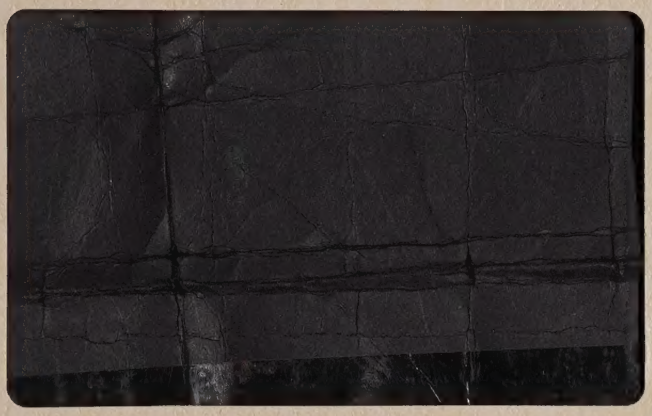

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USER'S REFERENCE MANUAL

MODEL PI-210

4-CHANNEL WORD GENERATOR

(P R E L I M I N A R Y)

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1.0 General Description

The PI-210 word generator is a plug-in unit designed to operate in the Tektronix TM-500 series power modules equipped with Pulse Instruments MOD-200 custom inter-plug-in wiring. In addition, Pulse Instruments PI-100A 4-channel clock generator plug-in unit is required as the clock source. One PI-100A can drive up to a maximum of four PI-210 word generators in a given TM-500 series power module, giving a total of 16 channels of word outputs. The PI-210 will operate with input clock rates up to 30 MHz.

The PI-210 is organized as four 32-bit words. The four bits accessed at any given time appear at the front panel BNC connectors.

The word length of the channels can be programmed from 1 to 32 bits, inclusive, requiring all channels be the same length. However, if an odd number of bits is programmed, the maximum clock rate obtainable is 15 MHz, or 1/2 the maximum clock rate. This reduction in maximum clock rate occurs because each of the two RAMs used for storing data is always accessed at 1/2 the clock rate.

The word generator channels can also be cascaded to form longer word lengths up to 128 bits. The three cascading combinations available are:

Channels 1 and 2 cascaded only (1+2, 3, 4)
Channels 1 and 2 cascaded and Channels 3 and 4 cascaded (1+2, 3+4)
All Channels cascaded (1+2+3+4)

The longer word output always occurs at the last cascaded channel.

Each channel can be independently set for return to zero (RZ) or non-return to zero (NRZ) format by switches on the front panel. In addition, each channel can be independently set for complement ($\overline{\text{WORD}}$) or non-complement (WORD) output. When a channel is set for both RZ and $\overline{\text{WORD}}$, a return to one format occurs. This is particularly useful for generating "low true" enable pulses.

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2.0	Specification	
2.1	Architecture	
2.1.1	Number of channels	4 data channels plus 1 scope sync channel.
2.1.2	Serial Word Length per Channel	2-32 bits, programmable from front panel.
2.1.3	Cascading	4 channels of N bits (no cascading). 1 channel of 2N bits and 2 channels of N bits. 2 channels of 2N bits. 1 channel of 4N bits (128 bits max.). Where $2 \leqslant N \leqslant 32$
2.2	Clock Source	
2.2.1	Input Connections	4 clock channels (A, B, C and D) from a PI-100A are connected to each PI-210 internally via Pulse Instruments MOD-200 custom inter-plug-in wiring, installed in the power module. Four PI-210 word generators maximum in a given power module.
2.2.2	Clock Select	Each clock channel, $\overline{A}$, B, C or D, can be assigned to any one or more PI-210 word channels by front panel programming switches. Data is clocked out during the leading edge of clock B, C or D input and during the trailing edge of clock $\overline{A}$ input.
2.3	Clock Outputs	
2.3.1	Amplitude	2V min. from 50 ohms.
2.3.2	Rise and Fall Times	Less than 8ns into 50 ohms.
2.3.3	Minimum Pulse Width	$\geqslant$13ns.
2.3.4	Formats	RZ/NRZ and WORD/$\overline{\text{WORD}}$ independently selectable by each channel. RZ not valid for $\overline{A}$ clock input.
2.3.5	Insertion Delay	$\leqslant$30ns between corresponding edges of selected

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		clock and word channel outputs as measured from the front panel BNC connectors.
2.3.6	Output Skew	$\leqslant$7ns among channels within the same plug-in and selecting the same clock input. 3ns typical. $\leqslant$10ns among channels within the same power module and selecting the same clock input. 5ns typical. Output skews among any three channels can be adjusted to 0 or $\pm$ by using the B, C and D clock delays.
2.4	Scope Sync Output	Occurs as the $(4N)^{th}$ bit, where $2 \leqslant N \leqslant 32$ is the serial word length. 0.6V P-P from 50 ohms with 3.5V DC pedestal.
2.5	Data Input	
2.5.1	Serial Mode	Four independent 32-bit serial words, 1 byte of each serial word per entry.
2.5.2	Parallel Mode	Thirty-two 4-bit parallel words, one 4-bit parallel word per entry.

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3.0 Organization

The internal storage section of the word generator is divided into two sections. The first is the data word section. It stores the pattern which is to be output to the front panel BNC connectors. The second is the control word section. It stores information for the control functions, such as serial word length and configurations, etc. Each of these storage sections will be described in detail.

3.1 Data Words

The data pattern is stored in a 32 x 4 RAM array. Depending on the application, the RAM array can be thought of either as four 32-bit serial words, each of which is divided into 4 bytes of 8 bits each, or as thirty-two 4-bit parallel words. See figure 3-1.

3.2 Control Words

There are three 8-bit control words which store the instructions for controlling certain operations of the word generator. These instructions include serial word length selection (variable from 1 to 32 bits), internal word output control, serial data word cascading, input clock selection, output return to zero and output complement.

Upon power up, all bits of all control wordsare set to 0.

3.2.1 Control Word 1

Control word 1 contains the instructions for controlling the output configuration, output control mode, and serial word length, as shown in Figure 3-2.

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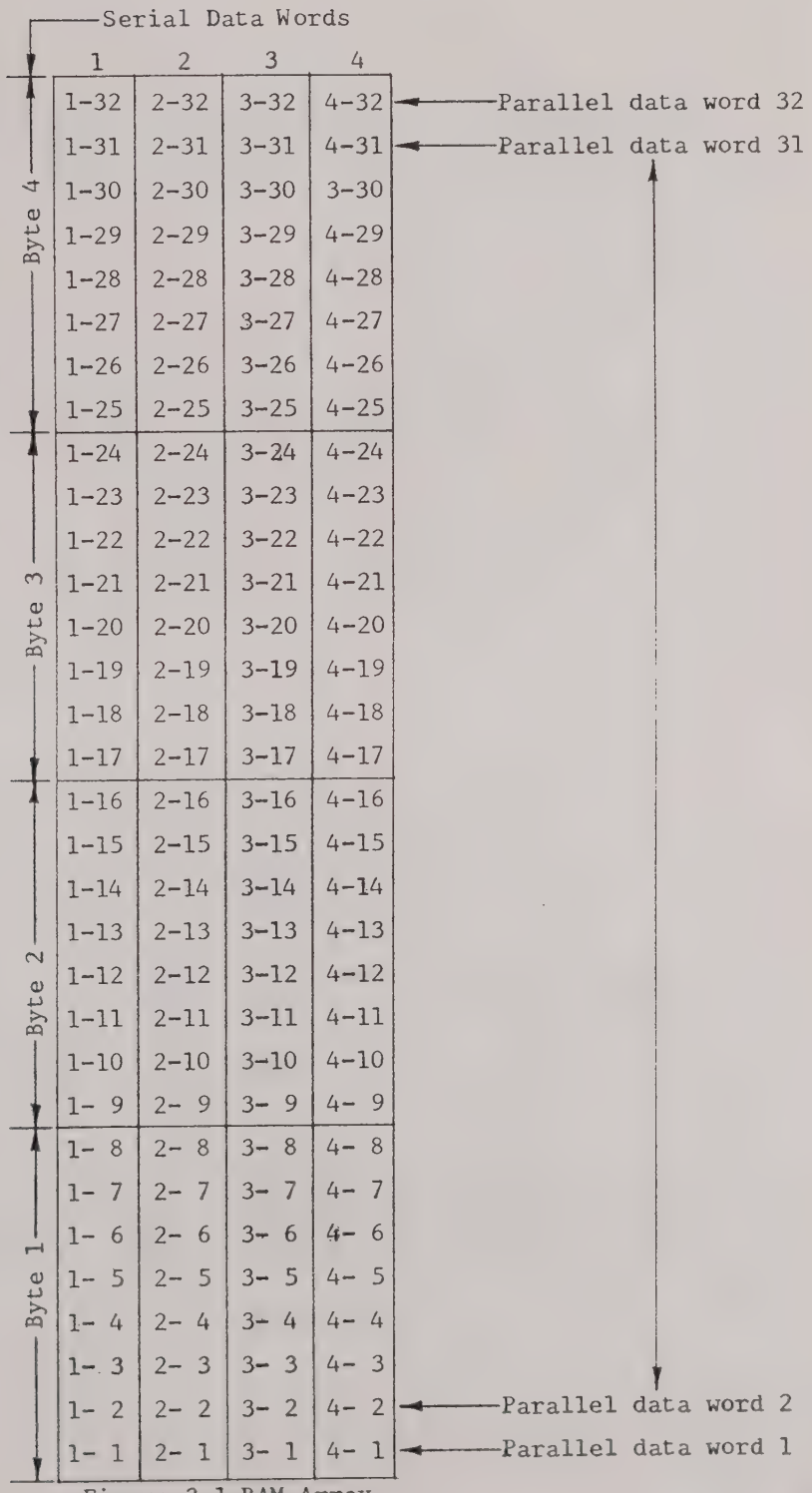

Figure 3-1 RAM Array

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Control Word 1							
Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
Cascading		OC	Serial Word Length				

Field Definitions

Cascading					
Bit 1	Bit 2	W1*	W2*	W3*	W4*
0	0	SDW1	SDW2	SDW3	SDW4
0	1	SDW1	SDW2+1	SDW3	SDw4
1	0	SDW1	SDW2+1	SDW3	SDW4+3
1	1	SDW1	SDW2+1	SDW3	SDW4+3+2+1

*W1 stands for output W1 on front panel, W2 for output W2, etc.

SDW= Serial Data Word

Bit 3	Output Control
0	Output controlledfrom front panel
1	Output controlledfrom control word 3

Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Serial Word Length
0	0	0	0	0	1 bit
0	0	0	0	1	2 bits
					...
1	1	1	1	0	31 bits
1	1	1	1	1	32 bits

Figure 3-2 Control Word 1

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3.2.1.1 Cascading

Bits 1 and 2 of control word 1 control the output cascading feature. This feature allows the serial data words to be cascaded at the output. For both bits 1 and 2 low (00), there is no cascading. For bit 1 low and bit 2 high (01), channels W1, W3 & W4 appear in a normal fashion, However, instead of the first bit of serial data word 2 appearing after the last bit of the same word, the first bit of serial data word 1 appears followed by the rest of serial data word 1. Following the last bit of serial data word 1 is the first bit of serial data word 2. Thus, serial data words 2 and 1 appear cascaded at channel W2.

For bit 1 high and bit 2 low (10) serial data word 2 followed by serial data word 1 appear at W2, while serial data word 4 followed by serial data word 3 appear at W4. W1 and W3 appear normal.

For both bits 1 and 2 high (11) serial data word 2 followed by serial data word 1 appear at W2.

Also, serial data word 4 followed by 3, 2 and 1 appear in that order at W4, thus cascading all four serial data at one output. The outputs on W1 and W3 appear normal.

It should be noted that the return to zero and complement functions operate directly on the W1, W2, W3 and W4 outputs and not on the serial data words. Thus, serial data word 1 can appear in a non-return to zero, complemented format on output W1 while appearing in a return to zero, non-complemented format and cascaded with serial data word 2 on output W2.

It should also be noted that the PI-100A clock (B, C, D or $\overline{A}$) selected by control word 2 operates on the W1, W2, W3 and W4 outputs and not on the serial data words. This makes it possible for serial data word 1 to be clocked by clock B on output W1 and by clock C on output W2 when cascaded with serial data word 2.

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3.2.1.2 Output Control Bit

Bit 3 of control word 1 is used to select between front panel or control word 3 control over the output return to zero and complement functions. If bit 3 is 0 then these functions are controlled by the eight switches in the "DATA/OUTPUT CONTROL" section of the front panel. If bit 3 is 1 then the front panel switches have no effict on these functions and control is derived instead from control word 3. The format of control word 3 is explained in section 3.2.3.

3.2.1.3 Serial Word Length

Bits 4 through 8 of control word 1 select the serial word length of the serial data words seen on the outputs W1, W2, W3 and W4. When cascaded, W2 will be twice this length. W4 may be twice or four times the programmed serial word length when cascaded.

There is only one serial word length and it is the same for all outputs, except for cascading.

Bit 8 is the least significant bit with bit 4 the most significant. See Figure 3-2 for the exact format.

3.2.2 Control Word 2 (Address = 101XX)

Control word 2 is used to select a PI-100A clock for each word generator output. Each output can independently select clock B, C, D, or $\overline{A}$.

See Figure 3-3 for the exact format of control word 2.

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Control Word 2							
Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
W1 CLK		W2 CLK		W3 CLK		W4 CLK	

Note 1	Note 2	PI-100 Clock Selected
0	0	B
0	1	C
1	0	D
1	1	$\overline{A}$ (Note 3)

Note 1: For W1 bit 1, for W2 bit 3, for W3 bit 5, for W4 bit 7.

Note 2: For W1 bit 2, for W2 bit 4, for W3 bit 6, for W4 bit 8.

Not 3: Because of an internal race condition, return to zero is an illegal operation for any channel that is clocked by $\overline{A}$.

Figure 3-3 Control Word 2

3.2.3 Control Word 3 (Address = 110XX)

Control word 3 can optionally be used to control the output return to zero and complement functions instead of these functions being controlled from the front panel. For control word 3 to have control, bit 3 of control word 1 must be set to a 1, as explained in section 3.2.1.2.

There is a one to one correspondence between the switch positions on the front panel and the bit positions in control word 3 as to which positions control which function. For example, position 1 controls the return to zero function of W1 both on the front panel and in control word 3. See Figure 3-4 for the exact format.

To control the return to zero and complement functions from control word 3, set up the front panel for the desired output control, select control word 3 and load. Next select control word 1 and fetch. Set the switches to the positions indicated by the LEDs except for bit 3, which should be set to a 1. Then load. The output will now be controlled by control word 3. The exact control word loading procedure is covered in section 5.3.

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Control Word 3							
Return to Zero				Complement			
Bit 1 W1	Bit 2 W2	Bit 3 W3	Bit 4 W4	Bit 5 W1	Bit 6 W2	Bit 7 W3	Bit 8 W4

Return to Zero	
Bit x	Output Condition
0	Non return to zero
1	Return to zero

Complement	
Bit x	Output Condition
0	Non complement
1	Complement

Figure 3-4 Control Word 3

SIZE	CODE IDENT NO.	DRAWING NO.
		91000060
SCALE		SHEET 12

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4.0 Front Panel Controls

(1) Power - Indicates power is on.

(2) CW/DW - Selects whether a control word (CW) or a data word (DW) is to be loaded. For digital programming, option -002 provides a third position, "DP" for loading data.

(3) CW Select/DW Select - Selects control word 1(L,L), 2(L,H) or 3(H,L) or data word 1, 2, 3 or 4, depending on the setting of the CW/DW switch.

(4) DW Byte - Selects data word byte 1(L,L), 2(L,H), 3(H,L) or 4(H,H).

(5) RUN/PAR/SER - Selects run mode (word generator in operating mode), parallel word loading format or serial word loading format.

(6) Fetch/Load - Selects whether information in address location A_0 - A_4 is to be fetched and displayed by the eight LED's, or the information specified by switches 1 through 8 is to be loaded into the control word or data word location specified by switches A_0 - A_4.

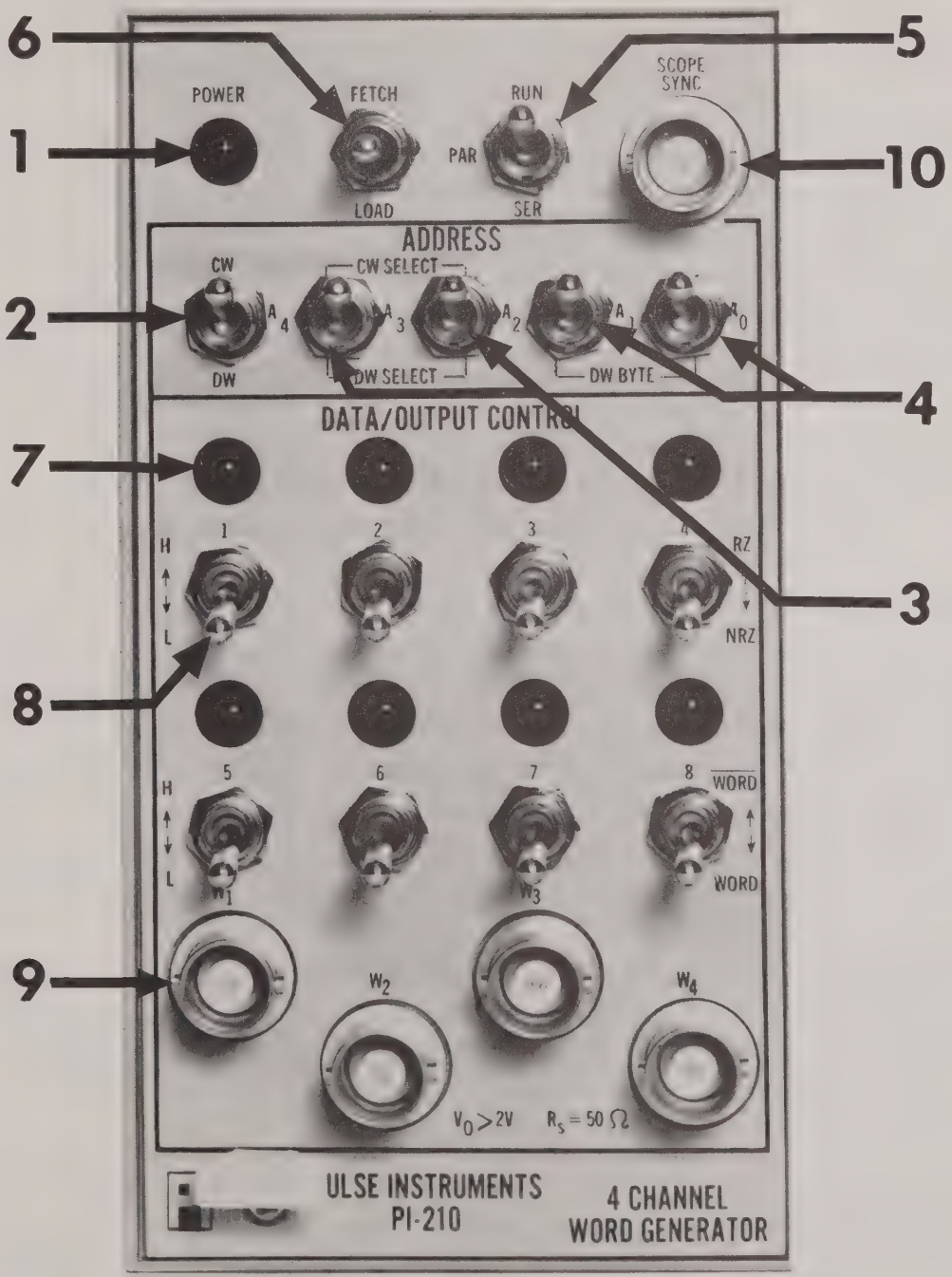
(7) Display LED (1-8) - Indicates information entered immediately after loading or information fetched.

(8) Dual Function Selector Switch - Switches 1-8 select word contents to be entered during loading. In RUN mode, switches 1-4 also select RZ or NRZ format, and switches 5-8 select $\overline{\text{WORD}}$ or WORD format for word channels W_1 - W_4, respectively. Switches 1-8 are inoperative in RUN mode if bit 3 in control word 1 is a 1.

(9) Word Output - Word output BNC connector. 2V minimum from a 50 ohm source.

(10) Scope Sync Output - Scope sync output BNC connector. 0.6V P-P from a 50 ohm source with 3.5V DC pedestal.

(3) BISHOP GRAPHICS, INC REORDER NO. 30501



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		91000060
SCALE		SHEET 14

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5.0 Loading

Data and control words are loaded via the toggle switches on the front panel and may be loaded in any order.

5.1 Loading Data Word in Parallel

When loading in the parallel mode, data is loaded as four bit parallel words. Each four bit parallel word corresponds to the data which will appear in parallel at the four BNC connectors when the location in which it is placed is accessed at a particular time while in the run mode. The total number of 4 bit parallel words is specified by the serial word length field of control word 1. The PI-210 can be programmed for up to 32 four bit parallel words.

The front panel markings which apply to the parallel mode of loading are written on a blue field.

To load data in parallel, first place the "RUN/PAR/SER" switch in the "PAR" position. Next, set the switches in the "ADDRESS" section to access the desired parallel word. See Figure 5-1 for the organization of the RAM in the parallel mode. Then place the first four switches in the "DATA/OUTPUT CONTROL" section (switches 1 through 4) to correspond to V 2.0 at the "W1" BNC when that address is accessed while in the run mode. In a similar fashion, switches 2 through 4 are used to load the data which will appear at W2, W3, and W4 respectively.

Last, the momentary contact "FETCH-LOAD" switch is placed in the "LOAD position. At that point data will be placed in RAM and also displayed on LEDs 1 through 4. The parallel words may be loaded in any order.

5.2 Loading Data Words Serially

When loading in the serial mode, the data for each serial data word is loaded serially, a byte (8 bits) at a time.

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Address Switches					Bit 1	Bit 2	Bit 3	Bit 4
A4	A3	A2	A1	A0				
1	1	1	1	1	Parallel Data Word 32			
1	1	1	1	0	Parallel Data Word 31			
1	1	1	0	1				
1	1	1	0	0				
1	1	0	1	1				
1	1	0	1	0				
1	1	0	0	1				
1	1	0	0	0				
1	0	1	1	1				
1	0	1	0	1				
1	0	1	0	0				
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0	1	0	0	0				
0	0	1	1	1				
0	0	1	1	0				
0	0	1	0	1				
0	0	1	0	0				
0	0	0	1	1				
0	0	0	1	0				
0	0	0	0	1	Parallel Data Word 2			
0	0	0	0	0	Parallel Data Word 1			

Figure 5-1 RAM array, Parallel Data Words

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The front panel markings which apply to the serial mode of loading are written on a red field. To load data serially, first place the "RUN/PAR/SER" switch in the "SER" position. Place the left most switch in the "ADDRESS" section to the "DW" (data word) position. Next, the two switches just to the right ("DW" SELECT"), are used to select the desired data word. Both switches in the down position (00) selects data word 1, 01 selects data word 2, 10 data word 3 and 11 selects data word 4. The two switches on the right side of the "ADDRESS" section ("DW Byte") select the desired byte. Both switches down (00) selects the first byte, 01 the second, 10 the third and 11 the fourth byte. See figure 5-2 for the organization of the RAM in the serial mode.

The desired data is entered via the eight switches in the "DATA/OUTPUT CONTROL" sections. When loading the first byte of any word, switch 1 corresponds to the 1st data bit out while in the run mode and switch eight corresponds to the 8th bit out. For the second byte, switch 1 corresponds to the 9th data bit in the data pattern while switch 8 corresponds to the 16th data bit. For the 3rd and 4th bytes switch 1 corresponds to the 17th and 25th data bits respectively.

The bytes may be loaded in any order. For instance, the fourth byte of serial data word three could be entered first, followed by the second byte of serial data word four, etc.

5.3 Loading the Control Words

The three control words can only be loaded in the serial mode. Each control word is one byte long. They may be loaded in any order.

To load a control word, first place the "RUN/PAR/SER" switch on the front panel in the "SER" position. Place the left most switch in the "ADDRESS" section to the "CW" (control word) position. Next, the two switches just to the right ("CW SELECT") are used to select the desired control word. Both switches in the down position (00) selects control word 1, 01 selects control word 2 and 10 selects control word 3. The 11 position is not used. The two switches on the right side of the "ADDRESS" section also are not used and may be in any position when loading the control words.

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Serial Data Words

	1	2	3	4
32 31 30 29 28 27 26 25 — Byte 4	Address = 10011	= 10111	= 11011	Address = 11111
24 23 22 21 20 19 18 17 — Byte 3	= 10010	= 10110	= 11010	= 11110
16 15 14 13 12 11 10 9 — Byte 2	= 10001	= 10101	= 11001	= 11101
8 7 6 5 4 3 2 1 — Byte 1	Address = 10000	= 10100	= 11000	Address = 11100

Figure 5-2 RAM Array, Serial Data Words

SIZE	CODE IDENT NO.	DRAWING NO. 91000060
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6.0 Operation

After the desired data and control words have been loaded, the unit is ready to run. This is done by placing the "RUN/PAR/SER" switch on the front panel in the "RUN" position. When this is done, the programmed data will appear at the BNC connectors on the front panel, provided the PI-100A in the left hand slot of the mainframe is enable.

As soon as the word generator is switched to the run mode, "CLOCK A" from the PI-100A plug-in will cause the RAM to be continuously addressed sequencially from the first location through the last location specified by the serial word length programmed in control word 1. Upon reaching the last location, the first location will be the next location addressed.

The RAM array actually consists of two 16 x 4 RAM devices. When in the run mode these RAMs are alternately accessed such that as data is being read out of one RAM the address of the next four bit word is being presented to the other RAM. Because the RAM devices are being alternately accessed, each RAM is being accessed at half the overall rate. Programming the serial word length for an odd number of words results in the same RAM being accessed for the last location and also for the first location, which is accessed immediately after the last location. For this reason, if the PI-210 is programmed for an odd word length the maximum input clock frequency is 15 MHz.

In the run mode, the eight switches in the "DATA/OUTPUT CONTROL" section exercise return to zero and complement control over the output, provided the output control bit (bit 3) of control word 1 is set to a 0, as described in sections 3.2.1.2 and 3.2.3.

If this bit is set to 0, then switches 1 and 5 control the return to zero and complement features respectively for channel W1. Switches 2 and 6 control the same features for channel W2, switches 3 and 7 for channel W3 and switches 4 and 8 for channel W4. For switches 1 through 4, the up position will cause the corresponding channel to operate in the return to zero format

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while the down postion will cause a non-return to zero format. The return to zero will occur on the high to low transition of the PI-100A clock selected for that channel. For example, if control word 1 is programmed such that channel W2 is clocked by PI-100A clock C, then the output of W2 will return to zero upon the high to low transition of clock C. Each channel may be operated in the return to zero format on the non-return to zero format independently of the other channels.

Switches 5 throgh 8 control the output complement format on channels W1 through W4 respectively. If the switch is up, the output will be complemented. A high programmed into a data word will appear as a low at the output if the complement format is selected.

If both the return to zero and complement format are selected for a given channel, then that channel will operate in a return to one format.

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7.0 Synchronizing two or more plug-ins

When two or more word generator plug-in units are operating in a common TM-500 series power module, it is often desirable to synchronize them so that the corresponding output bits from different plug-in units driven by a given PI-100A clock channel coincide in time.

The procedure for synchronizing two or more word generator plug-ins is as follows:

1. Disable the PI-100A clock generator by grounding the $\overline{\text{Clock INHB}}$ input BNC connector (use the BNC connector adapter-toggle switch fixture provided, or other equivalent means).

2. Set the RUN/PAR/SER switch of each PI-210 unit to PAR and address switches A_0 to A_4 all to zero (down). This clears all address counters.

3. Reset the RUN/PAR/SER switch of each PI-210 to RUN.

4. Enable the PI-100A clock generator by removing the input ground connection to the $\overline{\text{Clock INHB}}$ BNC connector. All PI-210 word generator plug-in units are now synchronized.

This procedure must be repeated whenever any PI-210 word generator is stopped and restarted, or whenever any PI-100A front panel toggle switch is changed after synchronization.

A similar procedure applies when the PI-100A is externally triggered, except that the disabling and enabling of the clock generator is accomplished by disconnecting and connecting the trigger input signal, respectively.

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8.0 Check out

The procedures in this section can be used for incoming inspection and, if necessary, periodic routine inspection. Since no precision timing or voltage levels are specified, no calibration is necessary. However, it may be desireable to run these check out procedures periodically if equiptment is used as part of a production test set-up.

Throughout this section standard hexadecimal (called hex for short) notation is used. See appendix C for an explanation of the hex system for representing binary numbers.

Hex notation will be used to specify the positions of the switches in the ADDRESS and DATA/OUTPUT CONTROL sections. The switch on the right hand side is defined as the least significant bit of the hex character.

To prevent confusion as to what is a hex number and what is not, all hex numbers will be preceeded by a colin. For example, :10 stands for the hex number "ten" which has a value of 16 if converted into its decimal equivalent. The use of the colin distinguishes it from a decimal ten or a binary two, both of which are written 10.

In the ADDRESS section there are five switches. This takes two hex characters to specify. For the hex number :XY, Y specifies the positions of switches A0 through A3. The position of the remaining switch, A4, is specifies by X. Thus :00 means all switches down, :1F all switches up and :03 means switches A0 and A1 up and A2, A3 and A4 down.

In the DATA/OUTPUT CONTROL section, hereafter refered to as DATA, there are two rows of four switches each. For the hex number :XY, Y specifies the positions of switches 1 through 4 and X specifies the positions of switches 5 through 8. Thus :03 means switches 1 through 6 down and switches 7 and 8 up.

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RUN, PAR, or SER will be used to specify the position of the RUN/PAR/SER switch. LOAD or FETCH will be used to specify the position of the LOAD/FETCH switch. Please note that this last switch is a momentary contact type.

8.1 Loading Test

The purpose of this test is to verify that the control words can be loaded correctly.

8.1.1 Control Word "Ones" Test

Load the following data in serial mode (SER):

ADDRESS	DATA	COMMENTS
:10	:FF	All DATA LEDs should be on.
:14	:FF	All DATA LEDs should be on.
:18	:FF	All DATA LEDs should be on.

8.1.2 Control Word "Zeros" Test

Load the following data in serial mode:

ADDRESS	DATA	COMMENTS
:10	:00	All DATA LEDs should be off.
:14	:00	All DATA LEDs should be off.
:18	:00	All DATA LEDs should be off.

8.2 Short Word Dynamic Test

The purpose of this test is to verify that the unit works dynamically.

8.2.1 Test Set up

A scope and a Pulse Instruments PI-100A are required for the rest of the tests in this procedure.

Make sure that the PI-100A and PI-210 are placed in mainframe slots designated for those plug ins.

Set the pulse width and delay of each of the four PI-100A clocks to

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minimum by setting the appropriate switches and turning all the appropriate knobs fully counterclockwise.

Next, connect CLKA of the PI-100A to one channel of the scope. Adjust the period of CLKA to 32 ns ± 1 ns. Then connect W1 of the PI-210 to another scope channel. Set the scope to trigger on the positive edge of an external signal and connect the external scope sync to the PI-210 SCOPE SYNC.

8.2.2 Channel Test

Load the following data in serial mode:

ADDRESS	DATA	COMMENT
:00	:80	lower byte DW1
:04	:90	lower byte DW2
:08	:A0	lower byte DW3
:0C	:B0	lower byte DW4
:10	:03	serial word length=4 bits

Set all channels for RZ and WORD. Place PI-210 in RUN mode. Now both PI-100A clock A and PI-210 channel W1 should be displayed on the scope. A high level should occur at W1 during one clock A cycle, followed by low levels for the next three clock A cycles. This is the 1000, or the :8 in the :80 which we programmed into DW1 above. The reason the output is :8 instead of :80 is that the serial word length is programmed for only 4 bits, the output would be a high level followed by seven lows, or :80.

Next give the PI-100A colck B delay control about ¼ to ¼ of a clockwise turn and then back to fully counterclockwise. The PI-210 W1 waveform should have moved to the right on the screen and then back again. Next turn the PI-100A clock B width control about ¼ to ½ of a clockwise turn and then back to fully counterclockwise. The falling edge of

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the PI-210 W1 waveform should have moved to the right and then back again.

Check for a :9 (1001) on channel W2, :A (1010) on W3 and :B (1011) on W4. As each of these channels is checked for correct data, check also control of delay and width of waveform by PI-100A clock B.

Display channel W1 on scope. Place switch 1 in the DATA section in the NRZ (down) position. The pulse width should increase. Place switch 5 in the WORD (down) position. The waveform should invert. Repeat the test using switches 2 and 6 for W2, 3 and 7 for W3 and 4 and 8 for W4.

8.2.3 Cascade Test

Load the following data in serial mode:

ADDRESS	DATA	COMMENT
:10	:43	DW2+DW1 on W2, serial word length=4

Set all channels for RZ and WORD. Place mode switch in RUN position. Display channel W2 on scope. Output should be one high, two lows, two highs, and three lows.(10111010 in binary or :BA in hex).

Load the following data in serial mode:

ADDRESS	DATA	COMMENTS
:10	:C3	DW2+DW1 on W2, DW4+DW3 on W4 serial word length=4

Set all channels for RZ and WORD. Place mode switch in RUN position. Display channel W4 on scope. Output should be one high, one low, three highs, one low, one high, one low, one high, two lows, two highs, and three lows (1011101010011000 in binary or :BA98 in hex).

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8.2.4 Clock Select Test

Load the following data in serial mode:

ADDRESS	DATA	COMMENTS
:10	:03	serial word length=4, no cascading
:14	:55	all channels clocked by PI-100A clock C

Set all channels for RZ and WORD. Place mode switch in RUN position. Display W1 on scope. Give the PI-100A clock C width control about ¼ to ½ of a clockwise turn and then back to fully counterclockwise. The falling edge of the PI-210 W1 waveform should have moved to the right and then back again.

Repeat the above test for PI-210 channels W2, W3, and W4.

Load the following data in serial mode:

ADDRESS	DATA	COMMENTS
:14	:AA	all channels clocked by PI-100A clock D

Check for delay and width control of W1, W2, W3 and W4 by PI-100A clock D.

Load the following data in serial mode:

ADDRESS	DATA	COMMENTS
:14	:FF	All channels clocked by PI-100A Clock A

All channels set for NRZ and WORD

Check for :8 on W1, :9 on W2, :A on W3 and :B on W4.

Load the following data in serial mode:

ADDRESS	DATA	COMMENTS
:14	:1B	W1-elock B, W2-clock C, W3-clock D W4-clock A

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All channels set for word, W1, W2, W3 set for RZ, W4 set for NRZ.

Check each channel for delay and width control as follows: clock B on W1, clock C on W2, clock D on W3. Check for correct data on W4 (:B) with no distortion.

8.3 Long Word Dynamic Check

This check tests all the data word RAM bits in insure that they can all be programmed.

8.3.1 Data Word "Ones" Test

Load the following data in serial mode:

ADDRESS	DATA	COMMENTS
:00	:FF	1st byte DW1
:01	:FF	2nd byte DW1
:02	:FF	3rd byte DW1
:03	:FF	4th byte DW1
:04	:FF	1st byte DW2
:05	:FF	2nd byte DW2
:06	:FF	3rd byte DW2
:07	:FF	4th byte DW2
:08	:FF	1st byte DW3
:09	:FF	2nd byte DW3
:0A	:FF	3rd byte DW3
:0B	:FF	4th byte DW3
:0C	:FF	1st byte DW4
:0D	:FF	2nd byte DW4
:0E	:FF	3rd byte DW4
:0F	:FF	4th byte DW4
:10	:1F	serial word length=32 bits

Set the scope for 100ns/division. View W1 on the scope. The waveform

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should always be in a high (one) state. Check W2, W3, and W4 to see that they are always in a high state.

8.3.2 Data Word "Zero Test"

Load the data as shown in the following table:

ADDRESS	DATA	COMMENTS
:00	:00	1st byte DW1
:01	:00	2nd byte DW1
:02	:00	3rd byte DW1
:03	:00	4th byte DW1
:04	:00	1st byte DW2
:05	:00	2nd byte DW2
:06	:00	3rd byte DW2
:07	:00	4th byte DW2
:08	:00	1st byte DW3
:09	:00	2nd byte DW3
:0A	:00	3rd byte DW3
:0B	:00	4th byte DW3
:0C	:00	1st byte DW4
:0D	:00	2nd byte DW4
:0E	:00	3rd byte DW4
:0F	:00	4th byte DW4

View W1 on the scope. The waveform should always be in a low (zero) state. Check W2, W3, and W4 to see that they are always in a low state.

8.3.3 Address Test

This test checks for the correct addressing of all the RAM bits.

Load the following data in serial mode:

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ADDRESS	DATA	COMMENTS
:00	:0F	1st byte DW1
:04	:0F	1st byte DW2
:08	:0F	1st byte DW3
:0C	:0F	1st byte DW4
:01	:12	2nd byte DW1
:05	:12	2nd byte DW2
:09	:12	2nd byte DW3
:0D	:12	2nd byte DW4
:02	:34	3rd byte DW1
:06	:34	3rd byte DW2
:0A	:34	3rd byte DW3
:0E	:34	3rd byte DW4
:03	:56	4th byte DW1
:07	:56	4th byte DW2
:0B	:56	4th byte DW3
:0F	:56	4th byte DW4

Set all channels for RZ and WORD.

Place mode switch in Run Position. Display channel W1 on scope with sweep set at 100ns/division. Output should be :0F123456 in hex (00001111000100100011010001010110 in binary).

Set channel W1 for WORD. Move waveform to top portion of scope screen. Display channel W2 on bottom portion of scope screen. Adjust the horizontal position of the two waveforms so that their peaks just touch. It can now be verified at a glance if W2 contains the same data as W1. If the two cables are not the same length, skew will exist between the displayed waveforms making verification more difficult.

Next connect W3 and then W4 to the channel which was connected to W2 and verify that they both contain the same data as W1.

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Appendix A, Data Word

I Loading Data Word Serially

A. Place "RUN/PAR/SER" switch on front panel in "SER" position.

B. Switch 1 in the "DATA/OUTPUT CONTROL" section of the front panel is used to load bit 1 (first byte), bit 9 (second byte), bit 17 (third byte) and bit 25 (fourth byte).

C. Serial Data Word 1: Address = 000XX
Serial Data Word 2: Address = 001XX
Serial Data Word 3: Address = 010XX
Serial Data Word 4: Address = 011XX
KL= Desired byte address (see below)

D. First Byte: Address = 0XX00
Second Byte: Address = 0XX01
Third Byte: Address = 0XX10
Fourth Byte: Address = 0XX11
MN= Desired serial data word address (see above)

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II Loading Data Word in Parallel

A. Place "RUN/PAR/SER" switch on front panel in "PAR" position.

B. Switch 1 in the "DATA/OUTPUT CONTROL" section of the front panel is used to load bit W1 of parallel data word, Switch 2 is used to load W2, 3 to load W3 and 4 to load W4. Switches 5 through 8 are unused during parallel loading.

Four Bit Parallel Word	Address
1st word	00000
2nd word	00001
-	-
31st word	11110
32nd word	11111

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Appendix B, Control Word

I Place "RUN/PAR/SER" switch on front panel in "SER" position.

Bit 1 of the control words is loaded via switch 1 in the "DATA/OUTPUT CONTROL" section of the front panel. Switch H= 1.

II Control Word 1: Address= 100XX

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
Cascading		OC	Serial Word Length				

A. Cascading

Bit 1	Bit 2	W1	W2	W3	W4
0	0	SDW1	SDW2	SDW3	SDW4
0	1	SDW1	SDW2+1	SDW3	SDW4
1	0	SDW1	SDW2+1	SDW3	SDW4+3
1	1	SDW1	SDW2+1	SDW3	SDW4+3+2+1

SDW= Serial Data Word

B. OC= Output Control (Return to zero and complement)

Bit 3	Output Control
0	Output controlled from front panel
1	Output controlled from control word 3

x= Don't care switch position

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SCALE		SHEET 32

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C. Serial Word Length

Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Serial Word Length
0	0	0	0	0	1 bit
0	0	0	0	1	2 bits
-	-	-	-	-	-
1	1	1	1	0	31 bits
1	1	1	1	1	32 bits

III Control Word 2: Address= 101XX

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
W1		W2		W3		W4	

Note 1	Note 2	Clock Selected
0	0	B
0	1	C
1	0	D
1	1	$\overline{A}$ (Note 3)

Note 1: for W1 bit 1, W2 bit 3, W3 bit 5, W4 bit 7.

Note 2: for W1 bit 2, W2 bit 4, W3 bit 6, W4 bit 8.

Note 3: Return to zero is an illegal mode of operation for any output selecting clock $\overline{A}$.

X= Don't care switch position.

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IV Control Word 3: Address= 110XX

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
W1	W2	W3	W4	W1	W2	W3	W4
Return to Zero				Complement			

Return to Zero	
Bit X	Output Behavior
0	Non-Return to Zero
1	Return to Zero

Complemented Output	
Bit X	Output
0	Non-complement
1	Complement

X= Don't care switch position

SIZE	CODE IDENT NO.	DRAWING NO.
		91000060
SCALE		SHEET 34

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Appendix C, Hexadecimal

Although somewhat confusing to the uninitated, hexadecimal (hex for short) is easily learned and greatly simplifies the programming of digital equiptment. For those already familiar with octal notation, hex is especially easy to learn, being only an extension of the 8 octal characters to a total of 16 characters.

Hex is a method of representing every four binary bits into one hex character. Thus an eight bit binary word can be represented by two hex characters, etc.

In the hexadecimal system, the appropriate decimal character is assigned to the binary number corresponding to its value. The binary number 1000, with the "1" being the most significant bit, would be represented by "8", which is the value of the binary number. This works fine up to and including a binary 1001 (a decimal 9). Beyond this we encounter a problem. If we go on using the decimal character for the next binary number, which is 1010, we would get adecimal 10 (ten). Since we wish to represent any combination of four binary bits as a single character we need to find 6 additional characters to represent binary numbers 1010 through 1111. Although any characters will do, the most logical ones are the first six letters of the alphabet: A,B,C,D,E and F. The resulting hexadecimal system is shown in figure C-1.

binary number	hex representation
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

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table continued

1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Figure C-1

Appendix D, Examples

A number of examples are given here to illustrate manual programming of the word generator. The main portion of the instruction manual should be consulted for detailed discussion of the instrument operation.

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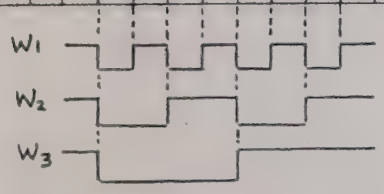
EXAMPLE 1 3-BIT SEQUENTIAL ADDRESS (SEE FIG 1 IN DATA SHEET, DS7A)

DATA/OUTPUT CONTROL SWITCHES

CONTROL WORD COMMAND

CW	A_4	A_3	A_2	A_1	A_0	1	2	3	4	5	6	7	8	
1	1	0	0	x	X	0	0	0	0	0	1	1	1	— NO CASCADING, FRONT PANEL CONTROL OF OUTPUT FORMAT, 8 BIT WORD LENGTH.
2	1	0	1	x	X	0	0	0	0	0	0	0	0	— CLOCK B INPUT TO ALL CHANNELS (CW*2 NEED NOT BE LOADED)
3	1	1	0	X	X	0	0	0	0	0	0	0	0	— FRONT PANEL CONTROL OF RZ/NRZ AND WORD/WORD FUNCTIONS (CW*3 NEED NOT BE LOADED)

SERIAL MODE	PARALLEL MODE																															
8	A_0			0	1	0	1	0	1	0					1	0	1	0	1	0	1				0	1	0	1				
7	A_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
6	A_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
5	A_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
4	A_4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
WORD LENGTH		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
SERIAL MODE	CW/CW ENC DW/DW SELEC A_4 A_3 A_2	BYTE 1								BYTE 2								BYTE 3								BYTE 4							
		A_1 A_0 = 0 0								A_1 A_0 = 0 1								A_1 A_0 = 1 0								A_1 A_0 = 1 1							
W_1	0 0 0	0	1	0	1	0	1	0	1																								
W_2	0 0 1	0	0	1	1	0	0	1	1																								
W_3	0 1 0	0	0	0	0	1	1	1	1																								
W_4	0 1 1																																



PI-210 PROGRAMMING WORK SHEET

SIZE	CODE IDENT NO.	DRAWING NO.
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SCALE		SHEET 37

EXAMPLE 2. OVERLAPPING FOUR PHASE CLOCK (SEE FIG. 3 IN DATA SHEET, DS7A)

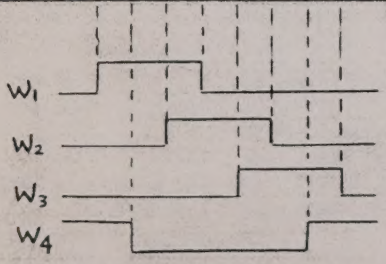
DATA/OUTPUT CONTROL SWITCHES

CONTROL WORD COMMAND

CW	A_4	A_3	A_2	A_1	A_0	1	2	3	4	5	6	7	8	
1	1	0	0	X	X	0	0	1	0	0	1	1	1	— NO CASCADING, CW#3 CONTROL OF OUTPUT FORMAT, 8 BIT WL.
2	1	0	1	X	X	0	1	0	1	0	1	0	1	— CLK C FOR ALL CHANNELS.
3	1	1	0	X	X	0	0	0	0	0	0	0	0	— NRZ AND WORD FOR ALL CHANNELS.

SERIAL MODE	8	PARALLEL MODE	A_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	7		A_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	6		A_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
	5		A_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
	4		A_4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
WORD LENGTH				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32

SERIAL MODE	CW/CW SELEC DW/DW SELEC A_4 A_3 A_2	BYTE 1	A_1 A_0 = 0 0	BYTE 2	A_1 A_0 = 0 1	BYTE 3	A_1 A_0 = 1 0	BYTE 4	A_1 A_0 = 1 1
W_1	0 0 0	1 1 1 0 0 0 0 0							
W_2	0 0 1	0 0 1 1 1 0 0 0							
W_3	0 1 0	0 0 0 0 1 1 1 0							
W_4	0 1 1	1 0 0 0 0 0 1 1							



PI-21C PROGRAMMING WORK SHEET

SIZE	CODE IDENT NO.	DRAWING NO. 91000060
SCALE		SHEET 38